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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/795,890	03/08/2004	Rinji Sugino	AF1216	2103

53104 7590 07/15/2005

THE CAVANAGH LAW FIRM
VIAD CORPORATE CENTER
1850 NORTH CENTRAL AVE., STE. 2400
PHOENIX, AZ 85004

EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/795,890	SUGINO ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group II (Claims 1-17) drawn to process of making a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 18-20 are cancelled.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Drawings

The drawings are objected to for the following reasons.

Figure 1 is not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of the Invention in view of U.S. Patent No. 6,780,741 to Chen et al.

Regarding to claim 1, Background of the Invention discloses a method for manufacturing a semiconductor component, comprising providing a semiconductor substrate 12 having a major surface 14; forming first and second surface features 20, 22 over the major surface 14; forming a first polysilicon layer 28 over the first and second surface features 20, 22 (pages 1 and 2, and fig. 1).

Background of the Invention doesn't disclose redistributing the first polysilicon layer in at least the region between the first and second surface features.

However, Chen disclose annealing the polysilicon layer (col. 3, lines 19-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the polysilicon layer in a hydrogen ambient, as taught by Chen in order to evolve into a small, random grain polysilicon layer, exhibiting smooth surfaces (col. 2, lines 25-28).

Regarding to claims 2 and 12, the method wherein redistributing the first polysilicon layer comprises annealing the first polysilicon layer (col. 3, lines 19-35).

Regarding to claims 3 and 17, the method wherein annealing the first polysilicon layer comprises nnnealing the first polysilicon in an ambient comprising hydrogen (col. 3, lines 19-35).

Regarding to claim 4, Background of the Invention in view of Chen discloses the claimed invention except for the annealing the first polysilicon layer includes heating the first polysilicon layer to a temperature ranging between approximately 750 degrees Celsius and approximately 1,100 degrees Celsius.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the first polysilicon layer that includes heating the first polysilicon layer to a temperature ranging between approximately 750 degrees Celsius and approximately 1,100 degrees Celsius, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding to claims 5 and 14, Background of the invention further includes forming a second polysilicon layer 34 over the first polysilicon layer 28 (page 2, and fig. 1).

Regarding to claim 6, Background of the invention in view of Chen does not disclose redistributing the second polysilicon layer. But Chen discloses annealing the polysilicon layer in a hydrogen ambient (col. 3, lines 19-33).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the polysilicon layer in a hydrogen ambient, as taught by Chen in order to evolve into a small, random grain polysilicon layer, exhibiting smooth surfaces (col. 2, lines 25-28).

Regarding to claims 7 and 15, the method wherein redistributing the second polysilicon layer includes annealing the second polysilicon layer in a hydrogen ambient (col. 3, lines 19-33).

Regarding to claims 8 and 13, Background of the invention in view of Chen discloses the claimed invention except for annealing the second polysilicon layer includes heating the second polysilicon layer to a temperature of at least 750 degrees Celsius.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the second polysilicon layer to a temperature of at least 750 degrees Celsius, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding to claim 9, Background of the Invention disclose a method for manufacturing a semiconductor component, comprising providing a semiconductor substrate 12 having a major surface 14; forming a first dielectric material 18 on the major surface; forming first and second conductors 20, 22 over first and second portions of the first dielectric material 18, the first and second conductors having a gap 24 therebetween; forming a second dielectric material 19 over the first and second conductors 20, 22; forming a first layer of polysilicon 28 over the first and second conductors 20, 22 (pages 1 and 2 and fig. 1). Background of the invention does not disclose repositioning atoms of the first layer of polysilicon.

Chen discloses annealing the polysilicon layer (col. 3, lines 19-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to anneal the polysilicon layer, as taught by Chen in order to evolve into a small, random grain polysilicon layer, exhibiting smooth surfaces (col. 2, lines 26-28).

Regarding to claim 10, Background of the Invention discloses the method wherein the first and second conductors comprises forming a second layer of polysilicon 34 over the first dielectric material 18; and patterning the second layer of polysilicon over the first dielectric material to form the first and second conductors 20, 22 (pages 1-2, and fig. 1).

Regarding to claim 11, Background of the Invention in view of Chen does not disclose the method wherein forming the first layer of polysilicon over the first and second conductors comprises forming a third dielectric material on the first and second conductors and forming the first layer of polysilicon on the third dielectric material.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the third dielectric material on the first and second conductors and forming the first layer of polysilicon on the third dielectric material since it would have been known in the art that forming the third dielectric material on the first and second conductors and forming the first layer of polysilicon on the third dielectric material.

Regarding to claim 16, the method wherein forming the first layer of polysilicon includes forming the first layer of polysilicon to have a thickness ranging between a monolayer of polysilicon and about 300 Angstroms (col. 5, lines 26-30).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can

normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran